H:A

Notice of Allowability	Application No.	Applicant(s)	
	10/699,797	NAGAO ET AL.	
	Examiner	Art Unit	
	Fetsum Abraham	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amt filed on 12/06/04*.

2. ☒ The allowed claim(s) is/are *27-29,33-35,39-47 and 51-56*.

3. ☒ The drawings filed on *02 September 2003* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. *10/145,033* .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Statement of reasons for allowance

Claims 27-29,33-35,39-47,51-56, have been allowed.

Although there have been few relevant circuits in the art closely related to the claimed invention, the interconnection of the three transistors in the claimed pulse output circuit in display circuit application and the output as a result of the interconnection has not been rendered obvious or taught by the prior arts.

To discuss few, the circuit in US 2002/0158666 has similar interconnections between transistors (202, 203 and 204) respectively as transistors (101, 102, 103) in the application. However, transistor (202) can only transmit "0" voltage upon turning on by the input signal at the gate. Therefore, the analogous power ground potential cannot be considered as the claimed "second signal input section" which has different values in composition.

PN: 6,686,899 discloses a closely related circuit in figure 10A. However, the VBIAS seems to only have the function of turning the NMOS1 and NMOS2 on and off rather than additional function beyond that. Although a valid argument can be presented to the effect that a gate voltage in essence is a turning on and off voltage with no other significant function, the fact that NMOS2's source/drain node is rather in contact with the Vin terminal instead of the VSS or ground terminal as in the claimed invention. Therefore, the voltage level at N2 variably depends on the value of VIN rather than on the constant ground potential as in the claimed invention.

Figure 2A in US 2005/0051802 on the hand can be considered a close art to the claimed invention, at least partially. However, the gate of transistor (151) is in contact

with a constant power voltage (VDD) rather than on variable voltage signal (CKA) as in the claimed invention. Besides, a different voltage (IN) turns on/off transistor (153) rather than a common signal for both transistors (151 and 153).

The front-page circuit in US 2003/0034806 is also another closely related configuration to the claimed invention. However, the Sample Pulse's connection to the gate of transistor (102) and the capacitors' ground node qualitatively separate it from the claimed invention in terms of performance.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fetsum Abraham whose telephone number is: 571-272-1911. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915.

Fetsum Abraham

8/16/05